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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/510,300	PARK ET AL.	
	Examiner	Art Unit	
	Thoi V Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Amendment filed May 17, 2004.

Accordingly, claims 1, 10, 15 and 20 were amended. Currently, claims 1-20 are pending in this application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over den Boer et al. (USPN 5,641,974) in view of Shimada et al. (USPN 5,877,830).

Re claim 1, as shown in Figs. 1 and 4-7, den Boer discloses a liquid crystal display (LCD) comprising:

a thin film transistor plate further comprising:

a gate line 7 on a first transparent substrate 19,

a first data line 5 (at left of Fig. 7) arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode 17 protruding from said gate line in an area where said data line crosses said gate line,

a thin film transistor 9 having a source electrode 15 (Fig. 1), 29 (Fig. 4) connected to the data line and a drain electrode 13 (Fig. 1), 31 (Fig. 4) separated from the source electrode wherein the source and drain electrodes confront each other,

a passivation layer 33 (Fig. 4) covering the thin film transistor wherein a contact hole 35 exposing a portion of the drain electrode is formed in the passivation layer, and

a pixel electrode 3 formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the first data line at a first end of the pixel electrode and asymmetrically overlaps a second data line 5 (at right of Fig. 7) at a second end of the pixel electrode opposite the first end;

a counter plate comprising a common electrode 49, a black matrix 55 (Fig. 6) including vertical extending regions 56 which are aligned with the data line 5; and

liquid crystals 45 injected and sealed between the thin film transistor plate and the counter plate,

wherein, re claims 3-5, the passivation layer is an organic passivation layer made of acryl (col. 6, lines 10-14) or made of BCB (col. 5, lines 57-58).

Den Boer discloses a LCD that is basically the same as that recited in claim 1 except for a color filter and a black matrix disposed on the counter plate, wherein the black matrix is partially overlapped with the data line.

As shown in Figs. 1 and 2, Shimada et al. discloses a LCD having a color filter plate 12 including a black matrix 13, a color filter 14 and a common electrode 15 on a second transparent substrate 12a (col. 5, lines 50-57),

wherein the black matrix of the color filter plate asymmetrically overlaps the data line of the thin film transistor plate, thereby the black matrix is partially overlapped with the data line so as to improve the aperture ratio of the display device (col. 6, lines 8-22).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD of den Boer with the teachings of Shimada et al. by forming on the counter plate a color filter to realize a color display and a black matrix partially overlapped with the data line to improve the aperture ratio of the display (col. 6, lines 19-22).

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over den Boer et al. (USPN 5,641,974) in view of Shimada et al. (USPN 5,877,830) as applied to claims 1 and 3-5 above, and further in view of Kobayashi et al. (USPN 5,847,792).

The LCD of den Boer as modified in view of Shimada et al. above includes all that is recited in claim 2 except for a location of the black matrix which is selected according to a direction of rubbing an alignment film. As shown in Figs. 19A and 19B, Kobayashi discloses a LCD comprising a black matrix 35, a common electrode 12 and an alignment film on a counter substrate 2, wherein the black matrix is formed in regions on the counter substrate opposed to the regions in which inversely tilted domains are apt to be caused to prevent light leakage (col. 12, lines 50-53 and col. 13, lines 50-59). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the LCD of den Boer with the teaching of Kobayashi by selecting a location where the black matrix overlaps the data line

according to a direction of rubbing an alignment film to prevent leakage current due to photoelectromotive force (col. 13, lines 57-59).

5. Claims 6, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over den Boer et al. (USPN 5,641,974) in view of Yoshino (USPN 5,358,810).

As shown in Figs. 1 and 4-7, den Boer discloses a liquid crystal display (LCD) comprising:

a thin film transistor plate further comprising:

a gate line 7 on a first transparent substrate 19,

a data line 5 arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode 17 protruding from said gate line in an area where said data line crosses said gate line,

a thin film transistor 9 having a source electrode 15 (Fig. 1), 29 (Fig. 4) connected to the data line and a drain electrode 13 (Fig. 1), 31 (Fig. 4) separated from the source electrode wherein the source and drain electrodes confront each other,

a passivation layer 33 (Fig. 4) covering the thin film transistor wherein a contact hole 35 exposing a portion of the drain electrode is formed in the passivation layer, and

a pixel electrode 3 formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the first data line at a first end of the pixel electrode and asymmetrically overlaps a second data line at a second end of the pixel electrode opposite the first end;

a counter plate comprising a common electrode 49, a black matrix 55 including vertical extending regions 56 which are aligned with the data line 5 and horizontal extending regions 57 which are aligned with the gate line to prevent the ambient light from penetrating the display on a second transparent substrate 51; and

liquid crystals 45 injected and sealed between the thin film transistor plate and the counter plate,

wherein, re claim 7, an overlap width w (Fig. 7) between the first data line and the pixel electrode and between the pixel electrode and the second data line is from about 0-2 micrometer (col. 11, Chart 1); and

wherein, re claim 9, the passivation layer is an organic passivation layer made of acryl (col. 6, lines 10-14) or made of BCB (col. 5, lines 57-58).

Den Boer discloses a LCD that is basically the same as that recited in claim 6 except for a color filter disposed on the counter plate.

As shown in Fig. 1, Yoshino discloses a LCD having a counter plate which comprises a black matrix 24 and a color filter 36 and can be mass-produced with a low cost so as to obtain a color display having a sufficient light-shielding effect (col. 2, lines 25-29 and 43-46).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD of den Boer with the teachings of Yoshino by forming a color filter plate so as to realize a color display having a sufficient light-shielding effect (col. 2, lines 25-29 and 43-46).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over den Boer et al. (USPN 5,641,974) in view of Yoshino (USPN 5,358,810) as applied to claims 6, 7 and 9 above, and further in view of Hanazawa et al. (USPN 5,953,083).

The LCD of den Boer as modified in view of Shimada et al. above includes all that is recited in claim 8 except for an overlap width between the pixel electrode and the first data line which is selected according to a direction of rubbing an alignment film.

As shown in Figs. 10-12, Hanazawa discloses a LCD in which an overlap width "a" between a pixel electrode 51(PE) and a data line 50a(X) is selected according to a direction of rubbing an alignment film 88 (col. 7, lines 40-61).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the LCD of den Boer with the teaching of Hanazawa by forming an overlap width between the pixel electrode and the first data line which is selected according to a direction of rubbing an alignment film so as to minimize the influence of the parasitic capacitance corresponding to the capacitive coupling between the pixel electrode and the data line (col. 7, lines 52-61).

7. Claims 10-12, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanagawa et al. (USPN 5,953,088) in view of Murade (USPN 6,388,721 B1).

Re claims 10 and 20, as shown in Figs. 5 and 10-12, Hanagawa discloses a LCD comprising:

a thin film transistor plate 83 further comprising:

a gate line 62 on a first transparent substrate 60 (col. 3, lines 45-48),

a data line 50a(X) arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode 63 protruding from said gate line in an area where said data line crosses said gate line,

a thin film transistor TR having a source electrode 50a(X) connected to the data line and a drain 78 separated from the source electrode wherein the source and drain electrodes confront each other,

a passivation layer 81 covering the thin film transistor wherein a contact hole 82 exposing a portion of the drain electrode is formed in the passivation layer, and

a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole (Fig. 12), the pixel electrode asymmetrically overlapping with the data line by a distance a according to an alignment direction of an alignment layer (Figs. 10 and 11);

a color filter plate 87 including a color filter 85 and a common electrode 86 on a second transparent substrate 84 (col. 3, lines 59-63); and

liquid crystals 90 injected and sealed between the thin film transistor plate and the color filter plate,

wherein a cut-off film 53a(SH) is formed under the data line 50a(X), said cut-off film being asymmetrically overlapped by the data line and being partially overlapped by the pixel electrode by a distance b according to an alignment direction, and wherein the cut-off film 53a(SH) is substantially overlapped by the data line 50a(X) in the data line direction (Figs. 10 and 11);

wherein, re claim 11, the passivation layer is an organic passivation layer (col. 5, lines 63-67);

wherein, re claim 12, the cut-off film 53a(SH) and the gate line 62 are formed on a same level (Figs. 11 and 12); and

wherein, re claim 14, the cut-off film 53a(SH) is formed at one side of the data line, said side selected according to a direction of rubbing an alignment film (Fig. 10 and col. 7, lines 40-61).

Hanazawa discloses a LCD that is basically the same as that recited in claims 10 and 20 except for a black matrix formed on the color plate.

As shown in Fig. 20, Murade discloses a LCD comprising a black matrix 6 formed on a second substrate 31, a pixel electrode 14, a data line 2, and a cut-off film 7 formed under the data line and overlapped by the data line and the pixel electrode.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD of Hanazawa with the teaching of Murade by forming a black matrix on the second substrate so as to prevent the display from being directly exposed to light and hence to obtain high quality images (col. 6, lines 16-27).

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hanagawa et al. (USPN 5,953,088) in view of Murade (USPN 6,388,721 B1) as applied to 10-12, 14 and 20 above and further in view of Hanazawa et al (USPN 6,400,427 B1) and den Boer et al. (USPN 5,641,974).

The LCD of Hanazawa et al. as modified in view of Murade above includes all that is recited in claim 13 except for an overlap region between the pixel electrode, the cut-off layer and the data line range has a width of between 2 micrometer and 4 micrometer.

As shown in Fig. 11 of USPN 6,400,427 B1, Hanazawa et al. discloses that a difference W2-W1 between the overlap width W2 between a cut-off film 53b and a pixel electrode 51 and the overlap width W1 between a data line 50 and the pixel electrode is set to be substancially equal to the film thickness of a layer insulation film 75, which is about 500 nm or .5 micrometer (col. 7, lines 66-67; col. 8, lines 1-5 and 58-60). Meanwhile, den Boer discloses that the overlap width w in Fig. 7 between a data line and a pixel electrode is about 0-2 micrometer (col. 11, Chart 1). Accordingly, if the overlap width W1 is 2 micrometer, W2 will be 2.5 micrometer.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the LCD of Hanazawa et al. with the teaching of den Boer by forming an overlap region between the pixel electrode, the cut-off layer and the data line range has a width of between 2 micrometer and 4 micrometer so as to obtain an excellent display characteristic.

9. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanazawa et al. (USPN 5,953,088) in view of Yamashita et al. (USPN 5,659,375).

As shown in Figs. 10-12, Hanazawa et al. discloses a method of fabricating a liquid crystal display having a transparent substrate 60 on which a gate line region and a data line region are defined, comprising:

simultaneously forming a gate line 62 in the gate region wherein a gate electrode 63 protrudes from the gate line, and a cut-off film 53a(SH) which is asymmetrically overlapped by the data line region according to an alignment direction of an alignment film (Figs. 10 and 11);

forming a data line 50a(X) in the data line region on the transparent substrate, wherein the data line crosses and is insulated from the gate line, and wherein a source electrode 50a(X) is formed at one side of the data line, and wherein a drain electrode 78 is formed which confronts and is isolated from the source electrode;

forming a passivation layer 81 covering the gate fine region, the data line region and the cut-off film, wherein a contact hole 80 exposing a portion of the drain electrode is formed in the passivation layer, (Fig. 12); and

forming a pixel electrode 51(PE) connected to the drain electrode through the contact hole on the passivation layer (Fig. 12), the pixel electrode being overlapped with the data line region according to the alignment direction of the alignment film, wherein the pixel electrode partially overlaps the cut-off film 53a(SH) by a distance b, and the cutoff film 53a(SH) is substantially overlapped by the data line 50a(X) in the data line direction (Figs. 10 and 11),

wherein, re claim 16, the passivation layer is an organic passivation layer (col. 5, lines 63-67); and

wherein, re claim 17, the cut-off film 53a(SH) and the gate line 62 are formed on a same level (Figs. 11 and 12).

Hanazawa et al. discloses a method of fabricating a liquid crystal display that is basically the same as that recited in claim 15 except for the pixel electrode being asymmetrically overlapped with the data line region.

As shown in Fig. 1, Yamashita et al. discloses a liquid crystal display comprising a pixel electrode 14 formed with portions overlapping a first data line 11b and a second data line 11a on both sides thereof, wherein a first overlap width between the first data line 11b and the pixel electrode 14 being larger than a second overlap width between the pixel electrode 14 and the second data line 11a so as to prevent the pixel electrode from being disturbed by the potentials of its adjacent data lines (col. 7, lines 17-24).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the method of Hanazawa et al. with the teaching of Yamashita et al. by forming the pixel electrode asymmetrically overlapping with the data line region to prevent the pixel electrode from being disturbed by the potentials of its adjacent data lines and hence to realize a good display with high contrast (col. 12, lines 9-15).

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hanagawa et al. (USPN 5,953,088) in view of Yamashita et al. (USPN 5,659,375) as applied to claims 15-17 above, and further in view of Hanazawa et al (USPN 6,400,427 B1) and den Boer et al. (USPN 5,641,974).

Hanazawa discloses a method of fabricating a LCD that is basically the same as that recited in claims 18 except for an overlap region between the pixel electrode, the

cut-off layer and the data line range has a width of between 2 micrometer and 4 micrometer.

As shown in Fig. 11 of USPN 6,400,427 B1 (US'427), Hanazawa discloses that a difference W2-W1 between the overlap width W2 between a cut-off film 53b and a pixel electrode 51 and the overlap width W1 between a data line 50 and the pixel electrode is set to be substantially equal to the film thickness of a layer insulation film 75, which is about 500 nm or .5 micrometer (col. 7, lines 66-67; col. 8, lines 1-5 and 58-60), so as to obtain an excellent display characteristic due to small reduction in contrast (col. 7, lines 56-65). In addition, den Boer discloses that the overlap width w in Fig. 7 between a data line and a pixel electrode is about 0-2 micrometer (col. 11, Chart 1) so as to obtain a high aperture display (col. 3, lines 23-25). Accordingly, if the overlap width W1 is 2 micrometer, W2 will be 2.5 micrometer.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the LCD of Hanazawa et al. with the teachings of Hanazawa et al. (US'427) and den Boer by forming an overlap region between the pixel electrode, the cut-off layer and the data line range has a width of between 2 micrometer and 4 micrometer so as to obtain an excellent display characteristic with high aperture display (Hazanawa, col. 7, lines 56-65 and den Boer, col. 3, lines 23-25).

11. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over den Boer et al. (USPN 5,641,974) in view of Yoshino (USPN 5,358,810) and Murade (USPN

6,388,721 B1) as applied to claims 6, 7 and 9 above and further in view of Yamashita et al. (USPN 5,659,375).

The liquid crystal display of den Boer et al. as modified in view of Yoshino and Murade above includes all that is recited in claim 19 except for a first overlap width between the first data line and the pixel electrode being larger than a second overlap width between the pixel electrode and the second data line.

As shown in Fig. 1, Yamashita et al. discloses a liquid crystal display comprising a pixel electrode 14 formed with portions overlapping a first data line 11b and a second data line 11a on both sides thereof, wherein a first overlap width between the first data line 11b and the pixel electrode 14 being larger than a second overlap width between the pixel electrode 14 and the second data line 11a so as to prevent the pixel electrode from being disturbed by the potentials of its adjacent data lines (col. 7, lines 17-24).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the method of Hanazawa et al. with the teaching of Yamashita et al. by forming the pixel electrode asymmetrically overlapping with the adjacent data lines to prevent the pixel electrode from being disturbed by the potentials of its adjacent data lines and hence to realize a good display with high contrast (col. 12, lines 9-15).

Response to Arguments

12. Applicant's arguments filed May 17, 2004 have been fully considered but they are not persuasive.

Re claim 6, Applicant argued that none of the cited references, singly or in combination, teaches or suggest "wherein the pixel electrode partially overlaps the first data line at a first end of the pixel electrode ... wherein the pixel electrode asymmetrically overlaps a second data line 5 at a second end of the pixel electrode opposite the first end. The Examiner disagrees with Applicant's remarks since Fig. 7 of den Boer et al. clearly shows that feature of the claimed invention (see the Office Action above).

Re claims 10 and 20, Applicant argued that none of the cited references, singly or in combination, teaches or suggest "wherein a cut-off film is formed under the data line, said cut-off film being asymmetrically overlapped by the data line and being partially overlapped by the pixel electrode according to an alignment direction, and wherein the cut-off film is substantially overlapped by the data line in the data line direction. The Examiner disagrees with Applicant's remarks since Figs. 10 and 11 of Hanagawa et al. (USPN 5,953,088) clearly show that feature of the claimed invention (see the Office Action above).

Finally, re claim 15, Applicant argued that none of the cited references, singly or in combination, teaches or suggest "forming a pixel electrode connected to the drain electrode through the contact hole on the passivation layer, the pixel electrode being overlapped with the data line region according to the alignment direction of the alignment film, wherein the pixel electrode partially overlaps the cut-off film, and the cutoff film is substantially overlapped by the data line in the data line direction. The Examiner disagrees with Applicant's remarks since Figs. 10 and 11 of Hanagawa et al.

(USPN 5,953,088) clearly show that feature of the claimed invention (see the Office Action above).

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thoi Duong

07/17/2004